What is claimed is:

1. A delay locked loop (DLL) comprising:

a delay line including an input for receiving an external clock signal, and multiple outputs for providing multiple delayed signals;

a selector connected to the multiple outputs for selecting one of the multiple delayed signals as an internal clock signal, wherein the multiple delayed signals have different delays in relation to the external clock signal; and

a command react circuit connected to the selector, the command react circuit capable of activating a command set signal for enabling the selector to select a different delayed signal among the multiple delayed signals based on a command signal.

2. The DLL of claim 1 further comprising:

a phase detector for comparing the external and internal clock signals to produce shifting signals; and

a controller connected to the delay line for adjusting an amount of delay applied to the external clock signal based on the shifting signals when the external and internal clock signals are not synchronized.

3. The DLL of claim 1, wherein delay line includes a plurality of delay stages connected in series, wherein one of the multiple outputs connects to an output of the next to last delay stage, wherein another output of the multiple outputs connects to an output of the last delay stage.

4. The DLL of claim 1, wherein the selector includes a multiplexor, the multiplexor including a plurality of inputs to receive the multiple delay signals and an output to provide the internal clock signal.

5. The DLL of claim 1, wherein the command react circuit includes:

a first input for receiving the command signal;

a second input for receiving a phase detect signal, the phase detect signal being deactivated when the external and internal clock signals are not synchronized; and

an output for providing the command set signal, wherein the command set signal is activated when the command signal is activated to enable the selector to select a different one of delayed signals before the phase detect signal is deactivated.

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6. A delay locked loop (DLL) comprising:

a plurality of delay stages for applying a first amount of delay to an external clock signal to generate a delayed signal;

a selector connected to the delay stages for receiving the delayed signal to provide an internal clock signal such that the external and internal clock signals are synchronized; and

a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal and a second input for receiving a phase detect signal, wherein the command react circuit causes the selector to change the first amount of delay to a second amount of delay when the command signal is activated.

7. The DLL of claim 6, wherein the command react circuit causes the selector to change the second amount of delay back to the first amount of delay when the phase detect signal is activated and the command signal is not activated.

8. The DLL of claim 6 further comprising:

a phase detector for comparing the external and internal clock signals to produce shifting signals; and

a controller connected to the delay stages for adjusting the first and second amount of delays based on the shifting signals when the external and internal clock signals are not synchronized.

9. The DLL of claim 6, wherein the first amount of delay is greater than the second amount of delay.

10. The DLL of claim 6, wherein the first amount of delay is smaller than the second amount of delay.

11. The DLL of claim 6, wherein a difference between the first and second amount of delays is equaled to a predetermined delay.

12. The DLL of claim 6, wherein the phase detect signal is activated when the external and internal clock signals are not synchronized.

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13. A delay locked loop (DLL) comprising:

a plurality of delay stages for applying an amount of delay to an external clock signal to generate a delayed signal;

a selector connected to the delay stages for receiving the delayed signal to provide an internal clock signal such that the external and internal clock signals are synchronized; and

a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal and a second input for receiving a phase detect signal, wherein the command react circuit causes the selector to decrease the amount of delay by a delay quantity when the command signal is activated.

14. The DLL of claim 13, wherein the command react circuit causes the selector to increase the amount of delay by the same delay quantity when the phase detect signal is activated and the command signal is not activated.

15. The DLL of claim 13 further comprising:

a phase detector for comparing the external and internal clock signals to produce shifting signals; and

a shift register for adjusting the amount of delays based on the shifting signals when the external and internal clock signals are not synchronized.

16. The DLL of claim 13, wherein the selector includes a multiplexor.

17. The DLL of claim 13, wherein delay quantity is equaled to a delay of at least one delay stage.

18. The DLL of claim 13, wherein delay quantity is equaled to a predetermined delay.

19. The DLL of claim 13, wherein the phase detect signal is activated when the external and internal clock signals are not synchronized.

20. The DLL of claim 13, wherein the command react circuit further including a third input for receiving a phase lock signal, the phase lock signal being activated when the external and internal clock signals are synchronized.

21. The DLL of claim 20, wherein the command react circuit causes the selector to increase the amount of delay by the same delay quantity when the phase lock signal is activated and the command signal is not activated.

22. A delay locked loop (DLL) comprising:

a plurality of delay stages for applying an amount of delay to an external clock signal to generate a delayed signal;

a selector connected to the delay stages for receiving the delayed signal to provide an internal clock signal, wherein the external and internal clock signals are synchronized; and

a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal and a second input for receiving a phase detect signal, wherein the command react circuit causes the selector to increase the amount of delay by a delay quantity when the command signal is activated.

23. The DLL of claim 22, wherein the command react circuit causes the selector to decrease the amount of delay by the same delay quantity when the phase detect signal is activated and the command signal is not activated.

24. The DLL of claim 22 further comprising:

a phase detector for comparing the external and internal clock signals to produce shifting signals; and

a shift register for adjusting the amount of delays based on the shifting signals when the external and internal clock signals are not synchronized.

25. The DLL of claim 22, wherein the selector includes a multiplexor.

26. The DLL of claim 22, wherein delay quantity is equal to a predetermined delay.

27. The DLL of claim 22, wherein the phase detect signal is activated when the external and internal clock signals are not synchronized.

28. The DLL of claim 22, wherein the command react circuit further including a third input for receiving a phase lock signal, the phase lock signal being activated when the external and internal clock signals are synchronized.

29. The DLL of claim 28, wherein the command react circuit causes the selector to decrease the amount of delay by the same delay quantity when the phase lock signal is activated and the command signal is not activated.

30. A delay locked loop (DLL) comprising:

a plurality of delay stages for receiving an external clock signal to generate a first and a second delayed signal;

a selector connected to the delay stages for selecting the first delayed signals to be an internal clock signal, wherein the external and internal clock signals are synchronized; and

a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal and a second input for receiving a phase detect signal, wherein the command react circuit causes the selector to replace the first delayed signal with the second delayed signal as the internal signal when the command signal is activated.

31. The DLL of claim 30, wherein the command react circuit causes the selector to replace the second delayed signal with the first delayed signal as the internal signal when the phase detect signal is activated and the command signal is not activated.

32. The DLL of claim 30 further comprising:

a phase detector for comparing the external and internal clock signals to produce shifting signals; and

a controller connected to the delay stages for adjusting the amount of delays based on the shifting signals when the external and internal clock signals are not synchronized.

33. The DLL of claim 30, wherein the first delayed signal is provided by a first number of delay stages, and the second delayed signal is provided by a second number of delay stages, wherein the difference between the first and second number of delay stages is equal to a predetermined delay.

34. The DLL of claim 30, wherein the first delayed signal is provided by a first number of delay stages, and the second delayed signal is provided by a second number of delay stages, wherein the first number of delay stages is greater than the second number of delay stages.

35. The DLL of claim 30, wherein the first delayed signal is provided by a first number of delay stages, and the second delayed signal is provided by a second number of delay stages, wherein the first number of delay stages is less than the second number of delay stages.

36. The DLL of claim 30, wherein the phase detect signal is activated when the external and internal clock signals are not synchronized.

37. The DLL of claim 30, wherein the plurality of delay stages are connected in series and include a common input to receive the external clock signal, wherein the first delayed signal is generated at an output of the last delay stage in the series, wherein the second delayed signal is generated by an output of the next to last delay stage in the series.

38. The DLL of claim 30, wherein the plurality of delay stages are connected in series and include a common input to receive the external clock signal, wherein the first

delayed signal is generated at an output of the last delay stage in the series, wherein the second delayed signal is generated by an output of another delay stage in the series.

39. The DLL of claim 30, wherein the command react circuit further comprising a third input for receiving a phase lock signal, the phase lock signal being activated when the external and internal clock signals are synchronized.

40. The DLL of claim 39, wherein the command react circuit causes the selector to replace the second delayed signal with the first delayed signal as the internal signal when the phase lock signal is activated and the command signal is not activated.

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41. A delay locked loop (DLL) comprising:

a plurality of delay stages for applying an amount of delay to an external clock signal to generate a first and a second delayed signal;

a selector connected to the delay stages for selecting the first delayed signal to be an internal clock signal, wherein the external and internal clock signals are synchronized;

a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal and a second input for receiving a phase detect signal, wherein the command react circuit causes the selector to replace the first delayed signal with the second delayed signal as the internal clock signal when the command signal is activated, wherein the command react circuit causes the selector to replace the second delayed signal with the first delayed signal as the internal clock signal when the phase detect signal is activated and the command signal is not activated;

a phase detector for comparing the external and internal clock signals to produce shifting signals; and

a controller connected to the delay stages for adjusting the amount of delays based on the shifting signals when the external and internal clock signals are not synchronized.

42. The DLL of claim 41, wherein the first delayed signal is provided by a first number of delay stages, and the second delayed signal is provided by a second number of delay stages, wherein the difference between the first and second number of delay stages is equal to a predetermined delay.

43. The DLL of claim 41, wherein the first delayed signal is provided by a first number of delay stages, and the second delayed signal is provided by a second number of delay stages, wherein the first number of delay stages is greater than the second number of delay stages.

44. The DLL of claim 41, wherein the first delayed signal is provided by a first number of delay stages, and the second delayed signal is provided by a second number of delay stages, wherein the first number of delay stages is less than the second number of delay stages.

45. The DLL of claim 41, wherein the phase detect signal is activated when the external and internal clock signals are not synchronized.

46. The DLL of claim 41, wherein the delays stages are connected in series and include a common input to receive the external clock signal, wherein the first delayed signal is generated at an output of the last delay stage in the series, wherein the second delayed signal is generated by an output of the next to last delay stage in the series.

47. The DLL of claim 41, wherein the plurality of delay stages are connected in series and include a common input to receive the external clock signal, wherein the first

delayed signal is generated at an output of the last delay stage in the series, wherein the second delayed signal is generated by an output of another delay stage in the series.

48. The DLL of claim 41, wherein the command react circuit further comprising a third input for receiving a phase lock signal, the phase lock signal being activated when the external and internal clock signals are synchronized.

49. The DLL of claim 48, wherein the command react circuit causes the selector to replace the second delayed signal with the first delayed signal as the internal signal when the phase lock signal is activated and the command signal is not activated.

50. A memory device comprising:
a plurality of inputs for receiving an external clock signal and a plurality of input signals;
an array of memory cells;
a command decode circuit connected to the inputs, the command decode circuit includes a decode output for providing a command signal to operate on the array of memory cells; and
a delay locked loop (DLL) connected to the decode output, the DLL including:
a plurality of delay stages for applying a first amount of delay to the external clock signal to generate a delayed signal;
a selector connected to the delay stages for receiving the delayed signal to provide an internal clock signal, wherein the external and internal clock signals are synchronized; and
a command react circuit connected to the selector, the command react circuit including a first input for receiving the command signal and a second input for receiving a phase detect signal and a command

react circuit output for providing a select signal, wherein the command react circuit causes the selector to change the first amount of delay to a second amount of delay when the command signal is activated by certain combination of the inputs signals.

51. The memory device of claim 50, wherein the command react circuit causes the selector to change the second amount of delay back to the first amount of delay when the phase detect signal is activated and the command signal is not activated.

52. The memory device of claim 50, wherein the command signal is activated to activate a row of memory cells.

53. The memory device of claim 50, wherein the command signal is activated to activate a column of memory cells.

54. The memory device of claim 50, wherein the command signal is activated during a refresh operation of the memory device.

55. A memory device comprising:
a plurality of inputs for receiving an external clock signal and for receiving a plurality of input signals;
an array of memory cells; and
a delay locked loop (DLL), the DLL including:
a plurality of delay stages for applying a first amount of delay to the external clock signal to generate a delayed signal;
a selector connected to the delay stages for receiving the delayed signal to provide an internal clock signal such that the external and internal clock signals are synchronized; and
a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal and a

second input for receiving a phase detect signal and an output for providing a select signal, wherein the command react circuit causes the selector to change the first amount of delay to a second amount of delay when the command signal is activated by certain combination of the inputs signals to access the memory cells.

56. The memory device of claim 55, wherein the command react circuit causes the selector to change the second amount of delay back to the first amount of delay when the phase detect signal is activated and the command signal is not activated.

57. The memory device of claim 55, wherein the command signal is activated to activate a row of memory cells.

58. The memory device of claim 55, wherein the command signal is activated to activate a column of memory cells.

59. The memory device of claim 55, wherein the command signal is activated during a refresh operation of the memory device.

60. A system comprising:
a processor; and
a memory device connected to the processor, the memory device including:
a plurality of inputs for receiving an external clock signal and a plurality of input signals;
an array of memory cells;
a command decode circuit connected to the inputs, the command decode circuit includes a decode output for providing a command signal to operate on the array of memory cells; and
a delay locked loop (DLL) connected to the decode output, the DLL including:

a plurality of delay stages for applying a first amount of delay to the external clock signal to generate a delayed signal;

a selector connected to the delay stages for receiving the delayed signal to provide an internal clock signal, wherein the external and internal clock signals are synchronized; and

a command react circuit connected to the selector, the command react circuit including a first input for receiving the command signal and a second input for receiving a phase detect signal and a command react circuit output for providing a select signal, wherein the command react circuit causes the selector to change the first amount of delay to a second amount of delay when the command signal is activated by certain combination of the inputs signals.

61. The system of claim 60, wherein the command react circuit causes the selector to change the second amount of delay back to the first amount of delay when the phase detect signal is activated and the command signal is not activated.

62. The system of claim 60, wherein the input signals are sent to the memory device by the processor.

63. The system of claim 60, wherein the command signal is activated to activate a row of memory cells.

64. The system of claim 60, wherein the command signal is activated to activate a column of memory cells.

65. The system of claim 60, wherein the command signal is activated during a read operation of the memory device.

66. The system of claim 60, wherein the command signal is activated during a refresh operation of the memory device.

67. A system comprising:

a processor; and

a memory device connected to the processor, the memory device including:

a plurality of inputs for receiving an external clock signal and for receiving a plurality of input signals;

an array of memory cells; and

a delay locked loop (DLL), the DLL including:

a plurality of delay stages for applying a first amount of delay to the external clock signal to generate a delayed signal;

a selector connected to the delay stages for receiving the delayed signal to provide an internal clock signal such that the external and internal clock signals are synchronized; and

a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal and a second input for receiving a phase detect signal and an output for providing a select signal, wherein the command react circuit causes the selector to change the first amount of delay to a second amount of delay when the command signal is activated by certain combination of the inputs signals to access the memory cells.

68. The system of claim 67, wherein the command react circuit causes the selector to change the second amount of delay back to the first amount of delay when the phase detect signal is activated and the command signal is not activated.

69. The system of claim 67, wherein the input signals are sent to the memory device by the processor.

70. The system of claim 67, wherein the command signal is activated to activate a row of memory cells.

71. The system of claim 67, wherein the command signal is activated to activate a column of memory cells.

72. The system of claim 67, wherein the command signal is activated during a read operation of the memory device.

73. The system of claim 67, wherein the command signal is activated during a refresh operation of the memory device.

74. A method of operating a delay locked loop, the method comprising:
generating multiple delayed signals by delaying an external clock signal;
selecting a first delayed signal among the multiple delayed signals to be an internal clock signal;
synchronizing the internal and external clock signals;
selecting a second delayed signal among the multiple delayed signals to be the internal clock signal when a command signal is activated;
selecting the first delayed signal to be an internal clock signal when the command signal is deactivated; and
synchronizing the internal and external clock signals.

75. The method of claim 74 further includes selecting a third delayed signal among the multiple delayed signals to be the internal clock signal when another command signal is activated.

76. The method claim of 74, wherein generating first and second delayed signals includes applying unequal amount of delays to the external clock signal.

77. The method claim of 74, wherein selecting a first delayed signals includes selecting a signal that is generated by applying a first amount of delay to the external clock, wherein selecting a second delayed signals includes selecting a signal that is generated by applying a second amount of delay to the external clock signal, wherein the first delay is greater than the second amount of delay.

78. The method claim of 74, wherein selecting a first delayed signals includes selecting a signal that is generated by applying a first amount of delay to the external clock, wherein selecting a second delayed signals includes selecting a signal that is generated by applying a second amount of delay to the external clock signal, wherein the first delay is smaller than the second amount of delay.

79. A method of operating a delay locked loop, the method comprising:

applying an amount of delay to an external clock signal to generate an internal clock signal;

adjusting the amount of delay until the external and internal clock signals are synchronized; and

reducing the amount of delay by a delay quantity when a command signal is activated and before the external and internal clock signals are detected as out of synchronism.

80. The method of claim 79 further includes:

increasing the amount of delay by the same delay quantity when the command signal is deactivated; and

adjusting the amount of delay until the external and internal clock signals are synchronized.

81. The method of claim 79, wherein reducing the amount of delay occurs before a phase detect signal is activated, wherein the phase detect signal is activated when the external and internal clock signal are not synchronized.

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82. A method of operating a delay locked loop, the method comprising:

applying an amount of delay to an external clock signal to generate an internal signal;

adjusting the amount of delay until the external and internal clock signals are synchronized; and

increasing the amount of delay by a delay quantity when a command signal is activated and before the external and internal clock signals are detected as out of synchronism.

83. The method of claim 82 further includes:

reducing the amount of delay by the same delay quantity when the command signal is deactivated; and

adjusting the amount of delay until the external and internal clock signals are synchronized.

84. The method of claim 82, wherein increasing the amount of delay occurs before a phase detect signal is activated, wherein the phase detect signal is activated when the external and internal clock signal are not synchronized.